12.2 A 10b 50MS/s Pipelined ADC with Opamp Current Reuse

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Low-power ADCs have been designed using power-saving techniques such as switched opamp [1, 2] and opamp sharing [3, 4, 5, 6]. Both operate with the same principle that opamp is active with a half duty during one clock phase. During the other clock phase, opamp is switched off, or shared with another stage. The switched-opamp scheme has a drawback of slow operating speed since the opamp power needs to be switched back on from the power-saving off state. Partial opamp switching is a trade-off between the turn-on speed and power consumption [2]. It requires the same number of opamps as the conventional design, and thus has no area saving. On the other hand, the opamp-sharing method saves both power and area using half the number of opamps, and also operating opamp with a half duty per each stage. That is, one opamp serves two stages as residue amplifiers during two different clock phases. However, the opamp-sharing system has a problem that the opamp input summing node is never reset. Therefore, the offset depends on the previous signal and it suffers from the 1/f noise [3]. Techniques such as feedback-signal polarity inverting [4] and dummy switch method [5] alleviate the non-resetting problem by alternating the signal polarity to compensate for the effect. To reset the summing node, two-stage opamp can also be used with two first (input) stages [6]. As in the switched-opamp case, turning off one input stage during the sampling phase while operating the other, can reduce power but the same transient problem remains.

The proposed ADC based on current-reusing opamp is similar to either the switched-opamp or opamp-sharing architecture, as shown in Fig. 12.2.1. The ADC is composed of S/H, two current-reusing blocks resulting in four-stages of MDACs, five sub-ADCs, and digital logic. MDAC1 and MDAC4 share the bias current, and so do MDAC2 and MDAC3. Each current-reusing block has two independent inputs, and summing nodes are reset with no power and area overhead. NMOS and PMOS complementary input pairs provide two inputs. Instead of turning off one input stage in each phase or sharing an opamp for two phases, this method reuses the opamp bias current for two stacked opamps. The opamps with NMOS input are used for the MSB stages while those with PMOS inputs are used for the LSB stages, since the MSB stages require higher gain and wider bandwidth. It is a standard pipelined ADC based on a tri-level 3b capacitor MDAC whose residue plot is shown in Fig. 12.2.2. Each MDAC uses 6 comparators, and thermometer-coded 3 capacitors with three reference levels, V_{REF}, 0, $-V_{REF}$, to provide 7 DAC levels.

Figure 12.2.3 explains the operation of the current-reusing concept. During one phase, the input signal is sampled on the N-input while the P-input amplifies residue. During this phase, the gate of the N-input stage is reset to the common-mode voltage V_{INC}, and it works as an active load for the P-input amplifier. During the other phase, the roles are switched. The N-input stage amplifies residue while the P-input stage is reset to the common-mode voltage V_{IPC}, and becomes an active load. Unlike the opamp-sharing method, the summing node can be reset. Furthermore since all the transistors operate always in saturation, there is no power turn-on delay as in the switched-opamp method. The opamp input node is separated from the capacitors during the sampling phase. This is to prevent the residue output settling from being delayed by the input common-mode resetting since the same output node is shared. This separation is mandatory in the opamp-sharing scheme, but not required in this approach. However, the delay in the output settling is caused by the non-zero time constant resulting from the sampling capacitance and the sampling switch resistance. Any reset delay error at the summing node can be amplified to the output with a gain of $g_{mI}/(g_{mI} \times \text{feedback factor})$, where g_{mL} is the active load trans-conductance, g_{mI} is the input trans-conductance, and the feedback factor is usually lower than the ideal 1/4 due to the opamp input capacitance.

Figure 12.2.4 shows a simplified current-reusing opamp. It is a gain-boosted opamp with capacitive common-mode feedback. Capacitive level shifting is also used to connect the main amplifier to the NMOS boost-amplifier input. The capacitive level shift operates similarly as in the capacitive common-mode feedback. During one phase, C_1 samples the estimated voltage difference, and during the other phase, C_1 refreshes C_2 with charge redistribution so that C_2 can hold the constant voltage. The advantage of this capacitive level shifting is that the N-input boosting amplifier can be used for boosting both N- and P-side cascode devices. The N-input amplifier is fast and saves power. One extra stack of the PMOS device reduces the available output voltage swing. In most low-power designs, transistor V_{DSAT} is small, and one extra V_{DSAT} drop does not reduce the signal swing significantly. This design uses a $1V_{PP}$ signal swing. Even though the summing node is reset in this design, the output node is not reset due to the output node sharing as in other designs. Therefore, twice the output swing should be considered for the worst-case settling in the design.

The prototype is fabricated in 0.18μm CMOS. The active die size is $1.1\times1.3mm^2$. When the supply is 1.8V, the common-mode voltage is 1V, and two references are 1.25V and 0.75V. The chip consumes 18mW (11mW for analog and 7mW for digital) at 50MS/s. Figure 12.2.5 shows the measured DNL and INL. The DNL is ±0.2LSB, and the INL is ±0.4LSB. The FFT plots of the 1MHz and 20MHz tones are shown in Fig. 12.2.6. The SNDR is measured to be very close to the SNR. The measured ENOB and SNDR are 9.2b/8.8b and 56.9dB/54.6dB for 1MHz and 20MHz inputs, respectively. The SFDR is typically 70dB/69dB for the same condition. The ADC works with little loss in the ENOB within the temperature range of 0° to 85°C with any combination of supply voltages from 1.62V to 1.96V. The die micrograph is shown in Fig. 12.2.7.

Acknowledgements:
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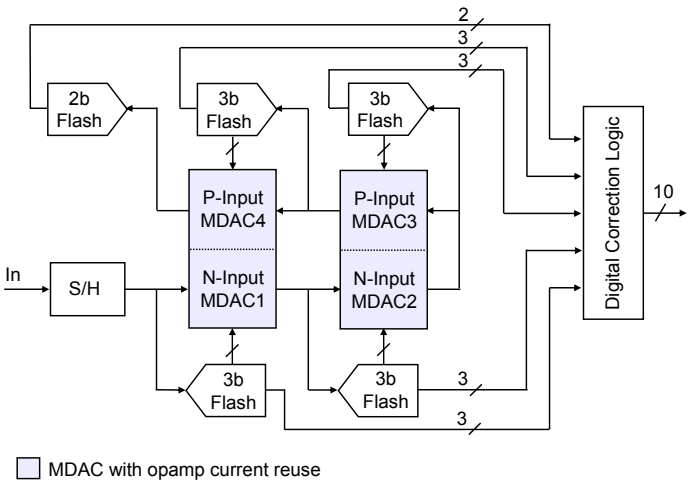

Figure 12.2.1: Block diagram of a 10b pipelined ADC with opamp current reuse.

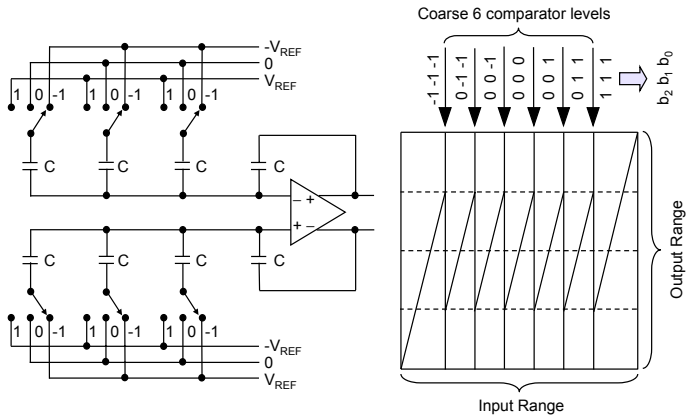

Figure 12.2.2: Tri-level 3b MDAC and its residue output.

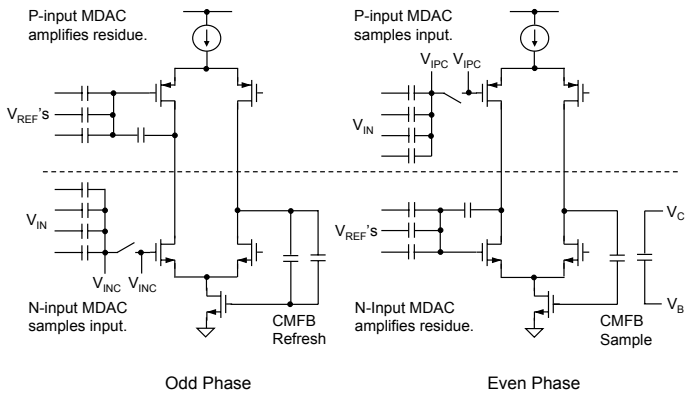

Figure 12.2.3: MDAC operation in both phases with simplified opamp schematic.

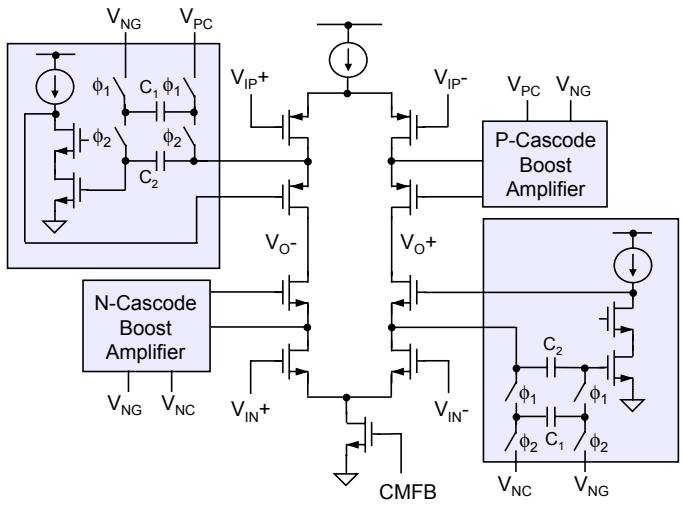

Figure 12.2.4: Opamp with both N and P inputs for current reuse.

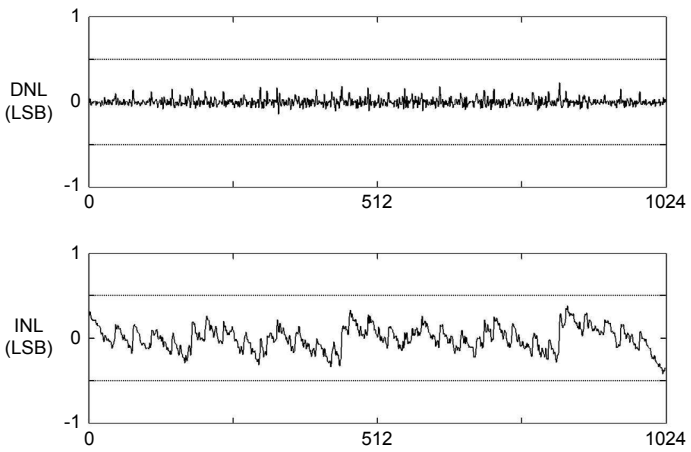

Figure 12.2.5: Measured DNL and INL.

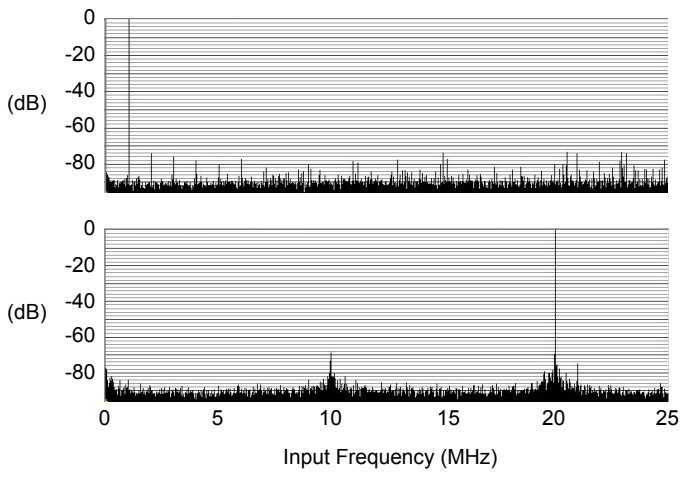

Figure 12.2.6: Measured FFT of 1MHz/20MHz tones sampled at 50MHz.

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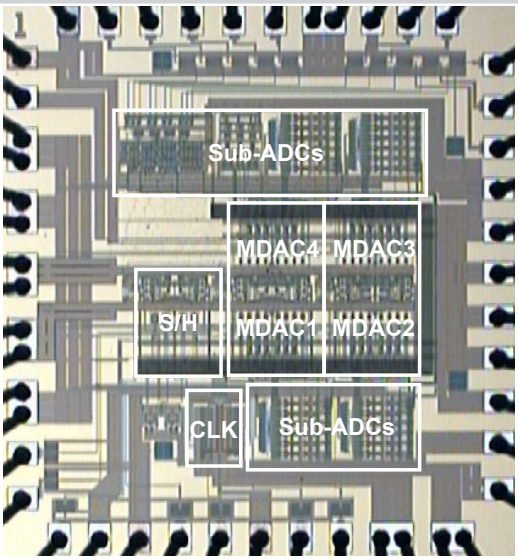

Figure 12.2.7: Chip micrograph.

